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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2008*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date *12/11/2008*.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.

DETAILED ACTION

Remarks

1.   This office action is in response to the amendment filed on 12/03/2008.

2.   Claim 29 has been amended.

3.   Claims 1-52 remain pending and have been examined.

Information Disclosure Statement

4.   The information disclosure statements filed on 12/11/2008 has been placed in the application file and the information referred to therein has already been considered.

Response to Arguments

5.   Applicant's arguments filed on 06/03/2008, in particular on pages 12-23, have been fully considered but they are not persuasive. For example:

- At page 13, first paragraph, Applicant submits that the language of claims 25, 26 and 46 is not indefinite, but is clear and definite. However, the Examiner respectfully disagrees. As the Applicant admitted, "at least one processor (i.e. <u>one or more</u>) comprises a plurality of processors (i.e. more than one)"[emphasis added] (Remarks, last line of page 12), it is clear that "at least one processor" has two situations either comprises one processor or more. For the case that only has one processor, it is unclear how the "one

processor" can comprise a plurality of processors. Therefore the 35 U.S.C. § 112 rejection to claims 25, 26, 46 and 47 is maintained.

- At page 13, second paragraph of section "Rejection of Claims Under 35 U.S.C. § 103(a)", Applicant submits that the cited prior art does not teach or suggest the limitation about selecting at least one of the plurality of memory devices to be updated using the update information. However, Examiner's position is that current invention discloses non-volatile memory which comprises multiple (different types) FLASH memory chips from the same or different manufactures and uses different access routines provided by the flash library to access and update code in those different types of memory chips. However, the claim language merely recites different type of memory devices which can be reasonable interpreted as different types of non-volatile memory or storage devices, e.g., disk drive, optical drive or other type storage/memory bank configuration that are not required physically or logically contiguous with one another and may be addressed using logically rather than physical addressing schemes. O'Neill discloses that non-volatile memory or storage area 1002 may include hard drives, optical drives, CD-writers, DVD-writers, tape drives, flash memory devices and EPROM devices (see for example, p.42, second paragraph). O'Neill also discloses the installation procedure validates and saves the update package 110 to non-volatile memory or storage on the client devices (see for example, p.25, second paragraph). Therefore, it is clear that in order to save the update

package, the type of the non-volatile memory has to be identified and

selected to indicated the target non-volatile memory type and location, i.e.

hard drivers, flash memory devices…

- At page 20, last paragraph, Applicant submits that O'Neill does not teach or

  suggest verifying the updating of the one of the at least one memory device

  using one of a CRC (Cyclic Redundancy Check) and O'Neill teaches that the

  "validation" takes place as a separate activity from the "updating" as recited in

  claim 5. However, Examiner respectfully disagrees. It should be noted that

  CRC (Cyclic Redundancy Check) validation is used to calculate the received

  update file and compare with the expected CRC value to verify and detect

  received file's error. As O'Neill disclosed, performing the validation checks

  (verifying) for the update package (the updating) using CRC (see for example,

  p.51) and saving the update package to the non-volatile memory (memory

  device (see for example, p.25), teaches the limitation as the applicant argued.

- At page 21, last paragraph to page 23 first paragraph, applicant submits that

  prior art O'Neill and Woodward do not teach the limitations as recited in

  claims 9 and 10. However, the Examiner's position is that as in Fig.10, step

  1210 "receive update", the FLASH 1002 receives update package via RAM

  by the operating system and accesses/writes update package to FLASH

  location 1224. Moreover, O'Neill also discloses FLASH accessing and

  referencing which is determined by the operating system or firmware of the

  electronic device (see for example, p.40, second paragraph). Woodward

further discloses a method to determine the manufacturers of flash memory

being used (see for example, col.8, lines 16-41). Therefore, combining

Woodward's method to determine the type/manufacturer of FLASH memory

and then using different methods to access said FLASH memory determined

by the operating system and firmware is obvious to the ordinary skills in the

art. Because different non-volatile memory/ROM requiring using different

access methods as disclosed by Woodstock (see for example, ABSTRACT

and col.4, lines 29-35).

- At page 25, forth paragraph, Applicant submits that O'Neill does not disclose

"...the flash memory comprises a plurality of flash memory chips". However,

Examiner's position is that non-volatile memory or storage area 1002 may

include hard drives, optical drives, CD- writers, DVD-writers, tape drives, flash

memory devices and EPROM devices [emphasis added](see for example,

p.42, second paragraph). The "flash memory devices" as disclosed above

certainly comprises a plurality of flash memory chips.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

7. Claims 25, 26 and 46-47 are rejected under 35 U.S.C. 112, second paragraph, as

being indefinite for failing to particularly point out and distinctly claim the subject

matter which applicant regards as the invention.

Claims 25, 26 and 46:

Claim 25, 26 and 46 recite at least one processor comprises a plurality of processor.

However, it is not clear how the "one processor" can comprise a plurality of

processors. For the purpose of compact prosecution, the Examiner reads it as –one

device comprise a plurality of processors---

Claim 47:

Claim 47 depends on claim 46. Therefore, it is also rejected for the same reason.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-24 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over

O'Neil (Patrick J. O'Neil, WO 02/41147 A1) in view of Woodward (James S.

Woodward, US 6,148,441).

Claim 1:

O'Neil discloses a method of updating non-volatile memory in an electronic device

via a communication network, the non-volatile memory comprising a plurality of

memory devices comprising a first memory device having a first associated type and

a second memory device having a second associated type, wherein the first

associated type and second associated type are not same (see for example, Fig.8A,

8B, "non-volatile memory" and related text; also see, p.40, first paragraph about type

of non-volatile memory/storage area: flash memory, disk drive, optical drive…), the

method comprising:

- receiving update information via the communication network (see for example,

  Fig.1B, item 110a-110c, "update package", "server manifest" and related text);

- selecting at least one of plurality of memory devices to be updated using the

  update information (see for example, p.15, second paragraph, "Upon recognition

  of one or more client devices 104a, 104b, 104c, the update server array 122 may

  transfer the server manifest to the one ore more client devices…") ;

- identifying updating software corresponding to at least the associated type of the

  at least one client device to be updated (see for example, p.15, The one or more

  client devices 104a, 104b, 104c then review the manifest and submit a request

  for the update package); and

- updating the at least one of the plurality of memory devices using the identified

  updating software and the update information (see for example, Fig.2A, step 216,

  "Install Update" and related text).

But O'Neil does not explicitly disclose identifying the associated type of the memory

devices. However, Woodward in the same analogous art of updating/reprogramming

non-volatile memory (Flash memory), discloses a method for determining the type of

flash memory being used (see for example, col.8, lines 16-41). Therefore, it would

have been obvious to one having ordinary skill in the art at the time the invention was made to use <u>Woodward</u>'s method to identify the type of non-volatile memory in the O'Neil client device. One would have been motivated to do so to use different interrupt routine according the type of memory to permits modification of the EISA configuration code in the flash memory while preserving the boot code and other code stored in the same sector of the memory array as suggested by <u>Woodward</u> (see for example, col.4, lines 29-35)

Claim 2:

<u>O'Neil</u> and <u>Woodward</u> disclose the method according to claim 1, <u>Woodward</u> further discloses determining the associated type of the at least one of the plurality of memory devices to be updated (see for example, col.4, lines 29-35)

Claim 3:

<u>O'Neil</u> further discloses the method according to claim 1, wherein the communication network is a wireless network (see for example, p.11, first paragraph, "wireless data transmission networks" and related text).

Claim 4:

<u>O'Neil</u> further discloses the method according to claim 1, wherein the communication network is a public network (see for example, p.11, first paragraph, "public internet", "public network" and related text).

Claim 5:

O'Neil also discloses the method according to claim 1, further comprising verifying

the updating of the one of the at least one memory device using one of a CRC, a

checksum, a hash code, and a digital signature (see for example, p.51, second

paragraph "These validation checks may include determining a cyclic redundancy

check code (CRC)" and related text).

Claim 6:

O'Neil discloses a method of updating non-volatile memory in an electronic device

via a communication network (see for example, Fig.8A, 8B, "non-volatile memory"

and related text), the non-volatile memory comprising a plurality of memory devices

comprising a first memory device having a first associated type and a second

memory device having a second associated type, wherein the first associated type

and second associated type are not same, (see for example, Fig.8A, p.40, first

paragraph about type of non-volatile memory/storage area: flash memory, disk drive,

optical drive...) the method comprising:

- communicating update information in an update package via the communication

  network from a management server to the electronic device (see for example,

  Fig.1B , item 112, "Update server array", item 110 "update package", items 104

  "Client device" and related text); and

- employing an update agent to interact with a memory library and the plurality of

  memory devices in non-volatile memory in the electronic device , and to identify

  updating software corresponding to at least an associated type of at least one of

  the plurality of memory devices.(see for example, Fig. 8B, item 1025 "Update

  agent", Fig.10, item 1004, 1222, p.52, "the update process commences with the

  update agent 1025 reading and executing instructions (memory library) contained

  in the update package stored in RAM memory section 1222 and related text)

But O'Neil does not explicitly disclose identifying the associated type of the memory

devices. However, Woodward in the same analogous art of updating/reprogramming

non-volatile memory (Flash memory), discloses a method for determining the type of

flash memory being used (see for example, col.8, lines 16-41). Therefore, it would

have been obvious to one having ordinary skill in the art at the time the invention

was made to use Woodward's method to identify the type of non-volatile memory in

the O'Neil client device. One would have been motivated to do so to use different

interrupt routine according the type of memory to permits modification of the EISA

configuration code in the flash memory while preserving the boot code and other

code stored in the same sector of the memory array as suggested by Woodward

(see for example, col.4, lines 29-35)

Claim 7:

O'Neil discloses the method according to claim 6, further comprising:

- employing a memory manager to access contents stored in plurality of memory

  devices, wherein the plurality of memory devices comprises a plurality of FLASH

  memory chips (see for example, Fig.2b, steps 262-280 about memory

  management and related text; also see p.24, last paragraph, "the current files

  stored in a first data area to a second data area (i.e. onboard flash memory";

  "compress files"); and

- employing the memory library to modify contents of the at least one FLASH

  memory chip (see for example, Fig.10, item 1004, 1222, p.52, "the update

  process commences with the update agent 1025 reading and executing

  instructions (memory library) contained in the update package stored in RAM

  memory section 1222 and related text) .

Claim 8:

O'Neil discloses the method according to claim 7, wherein the plurality of FLASH

memory chips are fabricated different manufacturers, and the plurality of FLASH

memory chips comprise one of a same amount of memory size and a different

amount of memory size (see for example, Fig8A, B, Fig.10, memory bank, item

1010, item 1012 address and size of memory bank. The flash memory/chips showed

in the Figures above have to be fabricated by the same or different manufacturer).

Claim 9:

O'Neil discloses the method according to claim 8, further comprising:

- determining which of the plurality of FLASH memory chips correspond to a particular FLASH memory modification (see for example, Fig.10, steps 1210-1280 and related text; also see p.48, "The code transformation is managed by the update agent 1025");

- employing an appropriate FLASH memory chip function (see for example, p.48, "process the instruction of the instruction set or update package 110"); and

- performing a corresponding FLASH memory modification (see for example, Fig.10, step 1230 "memory allocation", step 1240 "bank transfer" and related text).

Claim 10:

O'Neil further disclose the method according to claim 8, comprising

- employing the memory library by the update agent to permit access to and manipulation of a plurality of FLASH memory chips fabricated by different manufacturers chip (see for example, Fig.10, item 1004, 1222, p.52, "the update process commences with the update agent 1025 reading and executing instructions (memory library) contained in the update package stored in RAM memory section 1222 and related text) , and

- invoking appropriate functions stored in the memory library corresponding to the different manufacturers FLASH memory chips (see for example, p.48, "The code transformation is managed by the update agent 1025 which processes the instructions of the instruction set or update package 110").

But O'Neil does not explicitly disclose identifying the memory devices fabricated by

different manufacturers. However, Woodward in the same analogous art of

updating/reprogramming non-volatile memory (Flash memory), discloses a method

for determining the manufacturers of flash memory being used (see for example,

col.8, lines 16-41, "Intel ", "AMD"). Therefore, it would have been obvious to one

having ordinary skill in the art at the time the invention was made to use Woodward's

method to identify the type of non-volatile memory in the O'Neil client device. One

would have been motivated to do so to use different interrupt routine according the

type of memory to permits modification of the EISA configuration code in the flash

memory while preserving the boot code and other code stored in the same sector of

the memory array as suggested by Woodward (see for example, col.4, lines 29-35)

Claim 11:

O'Neil discloses the method according to claim 6, further comprising

- storing generic functions in the memory library which are employable by the

  update agent (see for example, Fig.10, item 1004, 1222, p.52, "the update

  process commences with the update agent 1025 reading and executing

  instructions (memory library) contained in the update package stored in RAM

  memory section 1222 and related text) ; and

- modifying contents of the at least one of the plurality of memory devices without

  identifying actual details regarding a specific memory device, wherein the actual

  details may be selected from a group comprising memory device manufacturer,

memory device type, memory size, memory model, and memory brand (see for

example, Fig.10 step 1224, "Apply update instructions" and related text) .

Claim 12:

O'Neil discloses the method according to claim 6, wherein the plurality of memory

devices are adapted to be grouped together, paired together, or arranged serially in

non volatile memory in the electronic device (see for example, Fig.10, item 1002

"flash" and item 1120, memory banks and related text).

Claim 13:

O'Neil discloses the method according to claim 6, further comprising creating a

memory map of memory device architecture (status table), the memory map

containing information selected from a group comprising of a number of memory

devices being employed by the electronic device, address ranges assigned to the

memory devices, memory device operating mode (the state of operation of the

devices), a map of data segments resident in the memory devices, and a map of

code segments resident in the memory devices (see for example, p.45, third

paragraph, "The status table 1050 is a data structure…and processing operations to

determine the state of operation of the devices") .

Claim 14:

O'Neil discloses the method according to claim 6, wherein the electronic device

comprises one of a mobile cellular phone handset, a personal digital assistant, a

pager, an MP3 (Moving Picture Experts Group Phase 1 Audio Layer 3) player, and a

digital camera (see for example, p.17, second paragraph, "cellular or mobile

phones).

Claim 15:

O'Neil discloses the method according to claim 6, further comprising employing an

update package status and reference section by the update agent code to retrieve

information regarding functions stored in a memory library code (see for example,

p.45, third paragraph, "The status table 1050 is a data structure...and processing

operations to determine the state of operation of the devices"; also see Fig.10, item

1004, 1222, p.52, "the update process commences with the update agent 1025

reading and executing instructions (memory library) contained in the update package

stored in RAM memory section 1222 and related text).

Claim 16:

O'Neil discloses the method according to claim 15, wherein the update package

status and reference section further comprises at least one of a status flag, starting

address, authentication value, location of update package, and locations of a

plurality of modification functions in non-volatile memory of the electronic device

(see for example, p.45, last paragraph, "the status table 1050 comprises one or

more flags...").

Claim 17:

O'Neil discloses the method according to claim 6, wherein the update package

comprises update information for at least one of firmware and software, version

upgrades, instructions to add new services, and instructions to delete services

employable in the electronic device (see for example, p.12, first paragraph, "a

version manifest which comprises a list of archived update package 110 including

operational software version information...").

Claim 18:

O'Neil discloses the method according to claim 6, further comprising employing a

boot initialization code to determine whether an update agent code is executed (see

for example, p.46, second paragraph, "This address refers to a section of the boot

block...").

Claim 19:

O'Neil discloses the method according to claim 18, wherein determining whether the

update agent code is executed comprises evaluating status information resident in

an update package status and reference section, and wherein if it is determined that

the update agent code is to be executed, then the update agent code accesses an

update package resident in the non-volatile memory of the electronic device by

employing an address of the update package stored in the update package status

and reference section (see for example, p.46, second paragraph, "The update agent

1025 checks the status table module 1050 to determine the value of the update state

variable to identify updating operations that should be performed or alternatively if no

operations are pending...")

Claim 20:

O'Neil discloses the method according to claim 6, wherein the update agent is

adapted to interact with the plurality of memory device as a single logical block of

non-volatile memory without distinguishing between specific memory devices (see

for example, Fig.9, step 1125- 1150, "updated bank storage" "apply update

instructions" and related text).

Claim 21:

O'Neil discloses the method according to claim 20, wherein the plurality of memory

devices are arranged according to one of contiguously or non-contiguously in

memory, and code and data resident in the memory devices are updateable by the

update agent regardless of which memory device the code and data reside in (see

for example, p.46, last paragraph, "the update management system utilizes a bank-

by-bank updating process for performing updates to the existing code version of an

electronic device") .

Claim 22:

O'Neil discloses the method according to claim 6, wherein the memory library is

adapted to accommodate a plurality of different types of memory devices by being

provided with drivers for the plurality of different types of memory devices during

manufacture (see for example, p.43, second paragraph, "the update agent 1025

includes one of more device drivers used during the updating processes.").

Claim 23:

O'Neil discloses the method according to claim 6, wherein the update agent is

adapted to accommodate a plurality of different types of memory devices by

accessing the memory library and compiling the update agent anew with drivers for

the plurality of different types of memory devices stored in the memory library during

manufacture (see for example, p.43, second paragraph, "the update agent 1025

includes one of more device drivers used during the updating processes.").

Claim 24:

O'Neil discloses the method according to claim 6, wherein the electronic device

comprises at least one processor, and wherein the at least one processor may be

associated with a specific memory device (see for example, Fig.10, item 1004, 1222,

p.52, "the update process commences with the update agent 1025 reading and

executing instructions (executed by processor) contained in the update package

stored in RAM memory section 1222 and related text).

Claim 32:

Claim 32 is a network/system version for performing the claimed method as in claim

10 addressed above, wherein all claimed limitation functions have been addressed

and/or set forth above and certainly a computer system would need to run and/or

practice such function steps disclosed by reference above. Thus, it also would have

been obvious.

10. Claims 25-27, 46-49 and 51-52are rejected under 35 U.S.C. 103(a) as being

   unpatentable over O'Neil (Patrick J. O'Neil, WO 02/41147 A1) in view of Gove (Gove

   et a;., US 5,471,592)

   Claim 25:

   O'Neil discloses the method as in claim 24 above, but does not explicitly disclose

   wherein the at least one processor comprises a plurality of processors and each of

   the processors is associated with a specific memory device. However, Gove in the

   same analogous art of multiprocessor system, discloses an image and graphic

   processor. The processor is structured with several individual processors all having

   communication links to several memories without restriction (see for example,

   ABSTRACT; also see Fig.1 item 100-103 processors and item 10, M1-Mj, memory).

Therefore, it would have been obvious to one having ordinary skill in the art at the

time the invention was made to incorporate Gove's method to O'Neil's system to

improve processor processing and memory accessing efficiency. One would have

been motivated to do so to handle multi-processor having multi-memories such that

the address space from all of the memories is available to one or more processors

concurrently even when the processors are handling different instruction sets as

suggested by Gove (see for example, col.2, lines 5-9)

Claim 26:

Gove further discloses the method according to claim 24, wherein the at least one

processor comprises a plurality of processors and the at least one memory device

comprises a plurality of memory devices, and wherein the plurality of processors are

adapted to share the plurality of memory devices (see for example, Fig.1, Fig.7 and

related text) .

Claim 27:

Gove further discloses the method according to claim 24, wherein the at least one

processor comprises a digital signal processor (DSP) adapted to execute DSP code

retrieved from at least one memory device (see for example, col.14, lines 47-64,

"Texas Instruments TMS 320 DSP processors").

Claims 46-48:

Claims 46-48 are network/system version for performing the claimed method as in

claims 25-27 addressed above, wherein all claimed limitation functions have been

addressed and/or set forth above and certainly a computer system would need to

run and/or practice such function steps disclosed by reference above. Thus, they

also would have been obvious.

Claim 49:

O'Neil discloses a mobile handset comprising:

- a flash memory (see for example, Fig.10, item 1002 "Flash" and related text) ;

  and

- an update agent capable of updating at least one of firmware and software

  resident in at least one of the plurality of flash memory chips (see for example,

  Fig.8B, item 1025 "update agent" and related text).

O'Neil further discloses the flash memory can be partitioned or logically divided into

a plurality of storage banks 1010 and the storage banks 1010 may be accessed

independently (see for example, p.40, second paragraph and p.42 second

paragraph, "the non-volatile memory or storage area 1002 may comprise numerous

types or configurations of storage space...").

But O'Neil does not explicitly disclose the flash memory comprises a plurality of flash

memory chips. However, Gove in the same analogous art of multi-processor system,

discloses a plurality of memory units (chips) (see for example, Fig.1, M0-Mj and

related text). Therefore, it would have been obvious to one having ordinary skill in

the art at the time the invention was made to use Gove's memory configuration to access different memory space independently and concurrently. One would have been motivated to do so to concurrently access and process memory information as suggested by Gove (see for example, col.2, lines 5-9)

Claim 51:

<u>Gove</u> also discloses the mobile handset according to claim 50, further comprising a plurality of processors, wherein each of the processors is adapted to manipulating a specific subset of the plurality of flash memory chips, and the plurality of processors are also adapted to employ the update agent to update at least one of firmware and software resident in at least one specific subset of flash memory chips (see for example, Fig.1, Fig.7 and related text).

Claim 52:

<u>O'Neil</u> discloses the mobile handset according to claim 49, further comprising:

- update at least one of firmware and software resident in at least one of the plurality of flash memory chips by executing update agent (see for example, fig.11, item 1314, "perform bank update" and related text; also see Fig.8B, item 1025 :update agent" and related text);

- execute update version of code resident in at least one of the plurality of flash memory chips (see for example, Fig.11, step 1320, "reinitiate client device" and step 1306, "processed to normal operation" and related text)

But O'Neil does not explicitly disclose assigning different processors to perform

update and execute the new updated software. However, as Gove disclosed multi-

processors system, it would have been obvious to one having ordinary skill in the art

at the time the invention was made to use different processor to perform different

task to provide a high degree of operational flexibility as addressed by Gove (see for

example, col.2, lines 50-59)

11. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Neil

(Patrick J. O'Neil, WO 02/41147 A1) in view of Gove (Gove et al., US 5,471,592) in

further view of Woodward (James S. Woodward, US 6,148,441).

Claim 50:

O'Neil further discloses the mobile handset according to claim 49, the mobile

handset further comprises a plurality of flash drivers, wherein the mobile handset is

adapted to employ an appropriate one of the plurality of flash drivers to update at

least a portion of at least one of firmware and software resident in at least one of the

plurality of flash memory chips (see for example, p.42, second paragraph, "the

update agent 1025 include one of more device driver used during the updating

processes").

But O'Neil does not explicitly disclose determine information regarding a type of

each of the plurality of flash memory chips at runtime. However, Woodward in the

same analogous art of updating/reprogramming non-volatile memory (Flash

memory), discloses a method for determining the type of flash memory being used

(see for example, col.8, lines 16-41). Therefore, it would have been obvious to one

having ordinary skill in the art at the time the invention was made to use <u>Woodward</u>'s

method to identify the type of non-volatile memory in the O'Neil and <u>Gove</u>'s client

device. One would have been motivated to do so to use different interrupt routine

according the type of memory to permits modification of the EISA configuration code

in the flash memory while preserving the boot code and other code stored in the

same sector of the memory array as suggested by <u>Woodward</u> (see for example,

col.4, lines 29-35)

12. Claims 28-31 and 33-45 are rejected under 35 U.S.C. 103(a) as being unpatentable

over O'Neil (Patrick J. O'Neil, WO 02/41147 A1)

Claims 28-31 and 33-45:

Claims 28-31 and 33-45are network/system version for performing the claimed

method as in claims 6-9 and 11-24 addressed above, wherein all claimed limitation

functions have been addressed and/or set forth above and certainly a computer

system would need to run and/or practice such function steps disclosed by reference

above. Thus, they also would have been obvious.

Conclusion

13.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

Applicant's arguments with respect to claims rejection have been considered, but they are not persuasive. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zheng Wei whose telephone number is (571) 270-1059 and Fax number is (571) 270-2059. The examiner can normally be reached on Monday-Thursday 8:00-15:00.

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is 571- 272-1000.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Z. W./
Examiner, Art Unit 2192

/Tuan Q. Dam/
Supervisory Patent Examiner, Art Unit 2192